Remarks

Acceptance and entry therefor of this responsive Amendment as well as favorable consideration of the present claimed subject matter is respectfully requested.

The format employed in this submission is consistent with the official USPTO test procedure regarding the submission of Amendments/Responses to certain Art Units including the Technology Center Art Unit in charge of the above-identified application. Information regarding this was received in the communication mailed, by the USPTO, December 20, 2002.

A number of revisions are being implemented in the present Specification that are of a minor formal nature. Acceptance and entry therefor of the same is respectfully requested.

The status of the claims now pending are given hereinabove. Claims 1 and 2 were amended in consideration of further clarifying the claimed subject matter including in terms of more clearly defining the invention over that taught by the reference, as cited in the outstanding art rejection. Specifically, the relationship between the recited "third line" with that of the "second line" and the "MOSFET," according to base claim 1 has now been further defined. The invention according to independent claim 1 now also calls for

> "said third line [to have] a first terminal connected electrically to said second line and a second terminal connected electrically to said MOSFET."

In independent claim 2, moreover, the intended connection effected between that of the "third line" and the "second line" and, also, with that of "a terminal of said circuit" has been further clarified/defined. Namely, the related

expression was amended to read as follows:

> "wherein said third line has a first terminal connected electrically to said second line and a second terminal connected electrically to said circuit."

It is submitted, the previously existing expression "said third line is used to connect ...," in claim 1, does imply a means by which a connection is effected between that of the "second line" and "a terminal of said MOSFET." Nonetheless, in consideration of further highlighting that featured aspect of the invention directed to the intent of the "third line", both claim 1 and that of claim 2 were revised accordingly. It should be noted, the "first line" and "second line" are shown by the second level wiring layers (e.g., M2) and the "third line" which is electrically separated (or electrically isolated) from the first line is shown by the first level conductive layer (e.g., M1), as one example thereof (see Figs. 2-8, although not limited thereto).

According to the outstanding Office Action, claims 1-3 were finally rejected under 35 USC §102(e) as anticipated by Hidaka (US 5,880,493). It will be shown, hereinbelow, the invention according to claims 1-3, as now amended, was neither disclosed by Hidaka nor, for that matter, could it have been suggested therefrom. Therefore, insofar as presently applicable, this rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

With regard to Hidaka's Fig. 13 layout/interconnection scheme, which is the layout configuration applied in the outstanding rejection, lines Lc2, Lb1 and FT7, allegedly, relate to the claimed "first line," "second line" and "third line," respectively, and are, also, are referred to as the "first interconnection (Lc2)," the "second interconnection (Lb1)" and the "third interconnection

(FT7)," respectively. According to independent claim 1, as now amended, the invention also calls for the "third line to [have] a first terminal connected electrically to said second line and a second terminal connected electrically to said MOSFET." Moreover, the invention according to independent claim 2, as now amended, also calls for the "third line to [have] a first terminal connected electrically to said second line and a second terminal connected electrically to said circuit." However, such is neither disclosed nor suggested by Hidaka.

With regard to Hidaka's Fig. 13 layout/interconnection scheme, it is noted that the third line (or interconnection (FT7)) is not shown to be electrically connected to the second line (or second interconnection (Lb1)), which is in clear contradistinction with that called for by the present claimed subject matter. For line Lb1, which is extended outside the array of unit areas (e.g., CC1, CC2), to be connected to a MOSFET (according to claim 1) or to a circuit (according to claim 2) within, for example, a unit area such as CC2 or CC1, in Fig. 13 of Hidaka, there must necessarily be a connection between the third line (FT7) and the second line (Lb1). Such, however, is not shown nor suggested by Hidaka, referring, as one example, to Hidaka's Fig. 13 arrangement which was applied in the rejection. It is submitted, for at least these reasons, the invention according to claims 1 and 2 and, therefore, also according to claim 3 (dependent on claim 2) is clearly defining thereover. That is, the invention according to claims 1-3, as now amended, not only was not disclosed by Hidaka but, also, was not suggested therefrom.

The Examiner's approval of the earlier submitted 'Proposal to Amend the Drawings', dated September 18, 2002, is noted. In view of the present requirement to submit corrected drawings thereto, concurrently filed herewith

is a paper entitled, 'Submission of Formal (Corrected) Drawings" together with a set of formal (corrected) drawings. Acceptance and formal entry therefor of the same is respectfully requested.

Therefore, in view of the Amendments and supportive discussion presented hereinabove, acceptance and formal entry therefor of this submission as well as favorable consideration of pending claims 1 - 3, as now amended, and an early formal Notification of Allowability of the above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.37426CX1) please credit any excess fees to such deposit account.

Respectfully submitted,
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Marked-Up Version Showing Changes Made

IN THE SPECIFICATION:

On Page 8, please **amend** the first full paragraph as follows:

Fig. 3 is a schematic device layout diagram showing one example illustrative of three cells which constitute the above-described circuit block. One or two P channel type MOSFETs (PchMOS) and one or two N channel type MOSFETs (NchMOS) are formed in their corresponding cell frames. Although the invention is not restricted in particular, the P channel type MOSFETs are placed on the upper side with the direction of each cell indicated by the character F as the reference, whereas the N channel type MOSFETs are similarly placed on the lower side. In the drawing, gate electrodes are respectively indicated by individual thick lines, and ~~diffused~~ diffusion layers are formed so as to interpose the gate electrodes interposed therebetween, whereby they are formed as source and drain regions. The relationship between the direction of such a cell and the placement of the P channel type MOSFETs (PchMOS) and N channel type MOSFETs (NchMOS) is similar to the following in all embodiments.

On Page 10, please **amend** the first full paragraph as follows:

The sources and drains of the N channel type MOSFETs or the sources or drains of the parallel-configured P channel type MOSFETs can be electrically connected to one another without the special interconnections M1 by forming ~~diffused~~ diffusion layers in common as in the case of the connections between the gate electrodes. In order to clearly represent the

MOSFETs constituting the cells in the same drawing, the respective MOSFETs are represented so that the sources and drains are respectively formed with the gate electrodes interposed therebetween.

On Page 10, please **amend** the paragraph beginning in the last line thereof and bridging to page 11, line 8, as follows:

The cells employed in the present embodiment represent those supplied with at least one input signal from other than the cells. In other words, a circuit in which signal transfer routes are formed by a plurality of logic gate circuits alone, even of circuits constructed of a plurality of logic gates as in a flip-flop circuit, a counter circuit and a comparator or the like as described above, more specifically, logic circuits constructed by only an electrical connection which shares the use of the ~~diffused~~ diffusion layers for the source and drain, and an electrical connection based on the wiring layer M1 corresponding to the first layer, can be regarded as one cell regardless of the size of the circuit scale.

On Page 12, please **amend** the second paragraph as follows:

The layout design of each random/logic circuit is performed as follows. After its circuit design, such a circuit is broken down into cells, which in turn are laid ~~but~~ out and placed, and the design of wiring between the cells can be automatically performed by a computer. However, when the number of interconnections provided in the central portion of the cell sequence is insufficient, the interconnections remain non-wired or a short circuit in other interconnections is developed. Accordingly, the conventional circuit layout

technology needs to re-layout the design of the cells in which wiring errors occur. However, the construction in which the slit cells are provided in the respective cells, as in the present embodiment, makes it possible to perform automatic wiring which selects such slit cells and is performed in combination with the wiring channels provided outside the cell sequence upon the occurrence of a shortage of input signal routes in the automatic wiring design, owing to the inputting of information that the wiring routes based on such slit cells exist.

On Page 19, please **amend** the last paragraph beginning in the penultimate line and bridging to page 20, line 13, as follows:

As a premise condition for using the source line in common, the cell pitch and the pitch of each contact CONT of a power supply portion are set to be identical to each other. Here, the cell pitch corresponds to the minimum pitch of each interconnection employed in the semiconductor integrated circuit. Upon automatic wiring, interconnections corresponding to second and third layers are formed according to the pitch referred to above. When the two cell sequences are placed back to back and the source line is used in common, the condition that the pitch of each contact is matched with the cell pitch, is additionally set. As a result, the contact CONT and each through hole TH provided on the source line shared between the two cell sequences placed back to back can be matched with each other. Here, the contact CONT indicates a portion for connecting ~~diffused~~ diffusion layers for the source and drain and a ~~diffused~~ diffusion layer for an ohmic contact formed in a well, and a metal wiring layer M1 corresponding to a first layer. The through

hole indicates a portion for connecting the metal wiring layer M1, corresponding to the first layer, and a metal wiring layer M2, corresponding to a second layer, to each other.

On Page 20, please **amend** the first full paragraph thereof as follows:

When each of the ~~diffused~~ diffusion layers formed on the left side with a gate electrode of each N channel type MOSFET interposed therebetween is set as the source, each power-supply cell comprised of the contact CONT and the through hole TH provided in association with the above-described cell pitch is formed in a ~~diffused~~ diffusion layer corresponding to the source and a P-type well region. A region corresponding to the drain is defined as a wiring region. Output interconnections each based on the metal wiring layer M1 corresponding to the first layer connected to the wiring channel (M2) formed outside along the cell sequence, for example, are formed in such a wiring region.

On Page 22, please **amend** the second full paragraph thereof as follows:

Figs. 9A and 9B are diagrams schematically illustrating a configuration of another embodiment of a dynamic RAM to which the present invention is applied. In the drawings, a schematic layout of ~~diffused~~ diffusion layers is shown in Fig. 9A, and a schematic layout of wiring layers is illustrated in Fig. 9B. In the layouts shown in the drawings, typical portions of respective circuit blocks constituting the dynamic RAM are illustrated so that their principal parts are understood. They are formed over a single semiconductor substrate,

such as monocrystal silicon, by a known semiconductor integrated circuit manufacturing technology.

On Page 23, please **amend** the first full paragraph thereof as follows:

In the present embodiment, a ~~diffused~~ diffusion layer for forming a stabilized capacitance is formed in the central portion of the semiconductor chip, where the wiring channel corresponding to the third layer and the wiring channel corresponding to the second layer intersect. Although the invention is not restricted in particular, the stabilized capacitance is used as stabilized capacitance of each de-boosting power circuit for producing operating voltages for the peripheral circuits. The de-boosting power circuits are constructed as follows. As will be described later, a plurality of circuits are placed so as to be distributed to a portion where peripheral circuits lying in the longitudinally-extending central portion on the semiconductor chip are formed. Further stabilized capacitance or capacitors having small capacitance values are also connected by utilizing spatial semiconductor regions of the peripheral circuits. Since such distributedly-provided stabilized capacitance or capacitors make use of the semiconductor regions limited as described above, they are set to a small capacitance value as compared with the stabilized capacitance formed in the chip's central portion.